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High Performance Buffer Amplifier for Liquid Crystal Display System

Arun Kumar*, Prof. Tarun Varma** and Dr. Rita Jain**

*PG Scholar, Department of Electronics and Communication Engineering, LNCT, Bhopal, (MP) India

**Assistant Prof., Department of Electronics and Communication Engineering, LNCT, Bhopal, (MP) India

***Prof. & HOD, Department of Electronics and Communication Engineering, LNCT, Bhopal, (MP) India

(Corresponding author: Arun Kumar)

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ABSTRACT: A high performance and buffer amplifier for liquid crystal display system is presented here. The proposed architecture contains self biased RAIL TO RAIL complementary differential pair , and class B output driving stage which is suitable for large and small size liquid crystal display, compensation capacitor and resistance are used to improve the settling time and slew rate of the buffer amplifier, an experimental prototype is shown here which is implemented in a .35 µm CMOS technology which draws only 8 µm static current and provide a settling time of 2.8 µs and rising and 3 µs during four the act area for the design of the buffer is 49 *60 µm With power supply of 3.3 it with stand with 1000 pF load capacitance.

I. INTRODUCTION

With incrementing ordinant dictation of high-speed high quality liquid crystal exhibit and market in recent years we have to match with these requisites to consummate the market demand and LCD driver generally contains shift registers, input register's, data latch, level shifter, digital to analog converter, Pre-Emphasis, and analog buffers the output buffer amplifier is vigorously affects the speed, resolution, voltage swing and power dissipation [12,4,8.9]. For each pixel we require a buffer amplifier so as the number of pixel increases the number of buffers to drive the to drive the panel increases, nowadays battery operated portable contrivances are acclimated to increment the performance and to elongate the battery life we require low-power high-speed buffer amplifier. LCD output buffer amplifier are realized by operational amplifier in unity gain configuration generally RAIL TO RAIL operational amplifiers are acclimated to get plenary output swing RAIL TO RAIL operation amplifiers are consist of complimentary differential amplifiers at first stage and a summing current source at second is stage with generally kenned as folded cascoded architecture then the output is stage which are this work in class B and class AB.

II. PROPOSED BUFFER DRIVING SCHEME

Generally introducing zero in transfer function of buffer amplifier using phase compensation register and output it makes the buffer stable but the slew rate is limited as due to small slew rate the settling time for large capacitive load will increased, means we have to suffer to achieve high-speed.

A typical two stage operational amplifier requires compensation for the stability some buffer amplifier's takes the output node as the dominant to achieve the stability without Miller capacitance [3,6] however charge conservation technique is commonly used in some LCD driver to reduce the dynamic power dissipation [1,2].

III. ZERO COMPENSATION TECHNIQUE

Zero compensation technique is generally used to get the dominant pole in buffer amplifier figure 1 shows a buffer amplifier with zero compensation. And fig 2 shows the configuration of proposed buffer amplifier using zero compensation technique. Fig. 4 shows the schematic of proposed buffer amplifier.

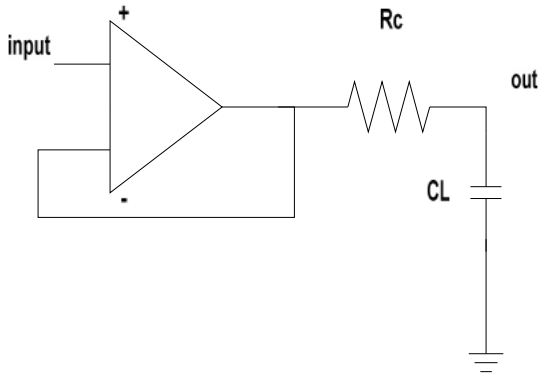

Fig. 1. Zero compensation buffer amplifier.

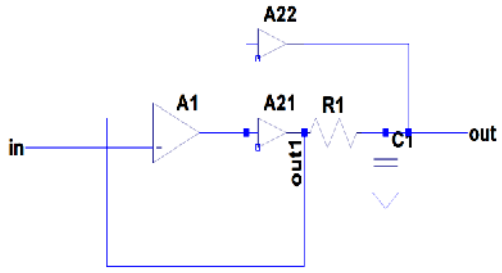

Fig. 2. Configuration of proposed driving method of buffer.

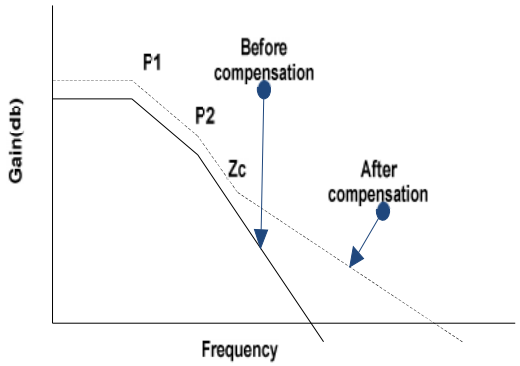

Fig. 3. Frequency response of buffer amplifier with dominant.

In figure 3 solid line shows frequency characteristic before compensation and dotted line after compensation, As dominant pole P1 shifted towards origin as with increasing load capacitance means gain bandwidth will decrease it also makes system unstable and degrade phase margin, for proper operation of buffer for high speed phase margin should be in between 70° to 45° generally they prefer 60° phase margin for high speed low-power buffer amplifier design here using "$R_C C_L$" introduces required phase margin, it introduce a zero in transfer function.

$$Z_C = \frac{-1}{R_C C_L}$$

This is called as zero compensation technique for large phase margin, it is generally used when we does not use them Miller capacitor in between differential amplifier and output is stage of differentiated amplifier. The value of zero located to left the most of unity gain bandwidth to the college RGB

$$\zeta = R_C\sqrt{C_L}$$

For 70° phase and margin $\zeta \geq 1$ and amplifier is stable, for ζ < .6 the phase margin is approximately given as I moved to women in

PM $\approx 100 \times \zeta$ and settling time = $\frac{4}{\zeta \omega_n}$

To get large phase margin R_C should be large but we can't increase the resistance R_C so much as it decreases the settling time, so there is compromise in between phase margin and settling time to get optimum phase margin.

As to account large capacitive load we have to increase the biasing current but it will increase the power loss in buffer amplifier, to solve on the issue to account the large capacitive load current dynamic current sensing technique is used to provide extra biasing current only during transition of input signal with the help of voltage divider method the current sensing technique sense the falling and rising edge according to that it provide the extra biasing current**.**

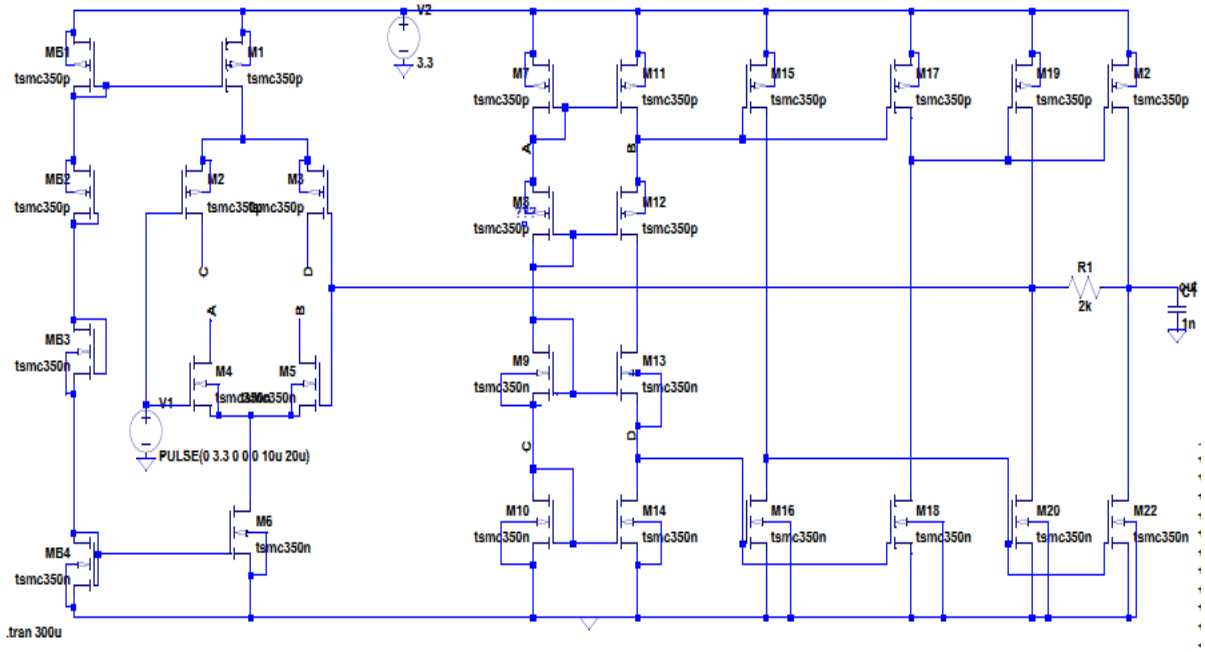

Fig. 4. Schematic of proposed buffer amplifier.

IV. SMALL SIGNAL ANALYSIS OF PROPOSED

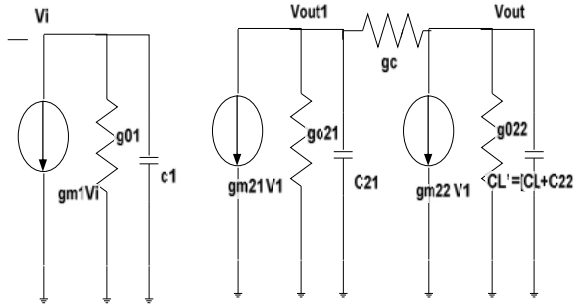

Fig. 5. Small signal model of proposed buffer.

The small signal of the proposed driving scheme is shown in figure 5 when we does not count the the transconductance of complimentary differential pair is gm1, and gm21, gm22 are the transconductance of two competitors, and g01, g021 and g022 are the output conductance, and and C_1, C_{21}, and C_{22}, are the paracetic capacitance. The open loop transfer function of the buffer,

$$A_0(s) = \frac{V_{out1}(s)}{V_i(s)} \approx A_{dc}\frac{\left(1-\frac{s}{Z_c}\right)}{\left(1-\frac{s}{P_1}\right)\left(1-\frac{s}{P_2}\right)}$$

where

$$A_{dc} = \frac{g_{m1}(g_{m21}g_c + g_{m21}g_{022} + g_{m22}g_c)}{g_{01}(g_cg_{021} + g_cg_{022} + g_{021}g_{022})}$$

$$\approx \frac{g_{m1}(g_{m2} + g_{m22})}{g_{01}(g_{021} + g_{022})}$$

$$P_1 = -\frac{(g_cg_{021} + g_cg_{022} + g_{021}g_{022})}{C'_L(g_{021} + g_c)}$$

$$\approx \frac{g_{021} + g_{022}}{C'_L}$$

$$P_2 = -\frac{g_{01}}{C_1}$$

$$Z_C = -\frac{(g_{m21}g_c + g_{m21}g_{022} + g_{m22}g_c)}{C'_Lg_{m21}}$$

The above Equivalent circuit contains contains three poles and zero the third pole is far away from other poles and zero, so it is neglected, g01, g021 and g022 conductance are much smaller than gc, the parasitic capacitance is also much smaller than load capacitance these approximations are taken for the analysis.

The closed loop transfer functiom of buffer,

$$A_{c1}(S) = \left(\frac{V_{out1}(s)}{V_i(s)}\right)_{closed\ loop} = \frac{A_{01}(s)}{1 + A_{01}(s)}$$

$$\approx \frac{\left(1 - \frac{s}{Z_c}\right)}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}}$$

the relation between Vout1 and Vout2 from the figure 5 is expressed as:

$$\frac{V_{out}}{V_{out1}} \approx \frac{1 + S\frac{g_{m22}C_{21}}{g_{m21}g_C + g_{m22}g_C + g_{m22}g_{021}}}{1 + S\frac{g_{m21}C_L}{g_{m21}g_C + g_{m21}g_{022} + g_{m22}g_C}}$$

the closed loop transfer function of overall block as shown in figure 4:

$$A_c(S) = \left(\frac{V_{out1}(s)}{V_i(s)}\frac{V_{out}(s)}{V_{out1}(s)}\right)_{closed\ loop}$$

$$= \frac{1 + S\frac{g_{m22}C_{21}}{g_{m21}g_C + g_{m22}g_C + g_{m22}g_{021}}}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}}$$

The zero from the data transfer function is neglected as it is far away from the dominant pole.

$$A_c(S) \approx \frac{1}{1 - s\left(\frac{1}{AP_1} + \frac{1}{Z_C}\right) + s^2\frac{1}{AP_1P_2}}$$

and it is equivalent to second o order transfer function so,

$$\omega_n = \sqrt{A_{dc}P_1P_2}$$

$$\zeta = -\frac{1}{2}\sqrt{A_{dc}P_1P_2}\left(\frac{1}{A_{dc}P_1} + \frac{1}{Z_C}\right)$$

$$\zeta \approx \frac{g_{m21}R_C}{2}\sqrt{\frac{g_{m1}C_L}{(g_{m21} + g_{m22})C_1}}$$

As from the above expressions damping factor ζ depends upon transconductance gm1, and the resistance of MOS using the push-pull output is stage depends upon the current flowing and push-pull stage With the use of dynamic bias sensor , we increase the biasing current during the transition phase of input this results in increase of transconductance gm1 and decreasing output resistance of push-pull stage during charging and discharging with load capacitance, as the settling time depends upon damping factor and natural frequency both this parameters increases with increasing transconductance of gm1 where gm1 is the transconductance of differential is stage, this results and decreasing the settling time means the response of buffer amplifier increases with the use of dynamic bias sensor.

V. DESIGN PARAMETERS OF RAIL-RAIL OPERATIONAL AMPLIFIER

process	.35 µm CMOS technology
Power supply	3.3 V
Load resistance	20 kΩ
Load capacitance	1000 pF
power dissipation	1mW
DC gain	95 db
Gain bandwidth product	1 MH
Phase margin	70°
Slew rate	5 V/ µs
Output voltage swing	0-3.3 V
input common mode range	0-3.3 V
Output stage	Class B

VI. SIMULATION RESULT

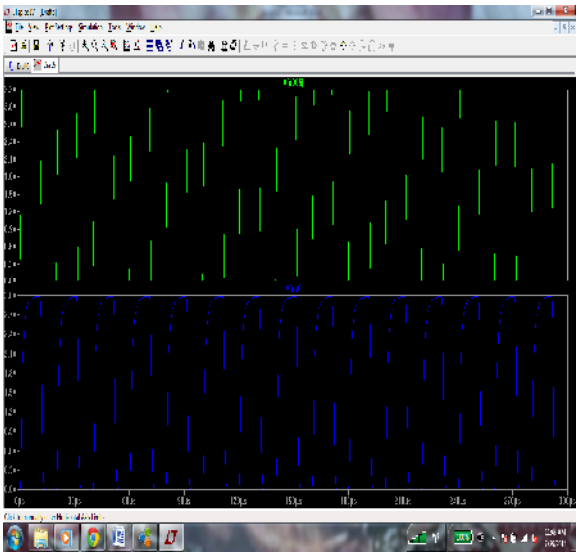

Fig. 6. Simulation result for step response.

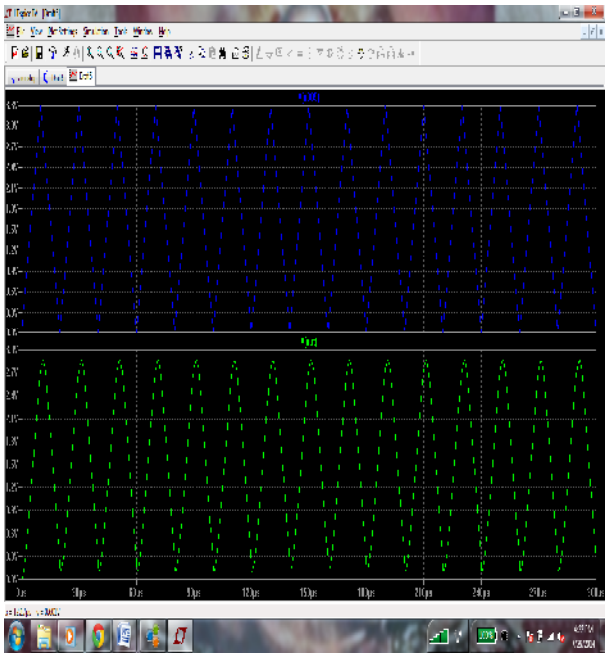

Fig. 7. Simulation result for triangular response.

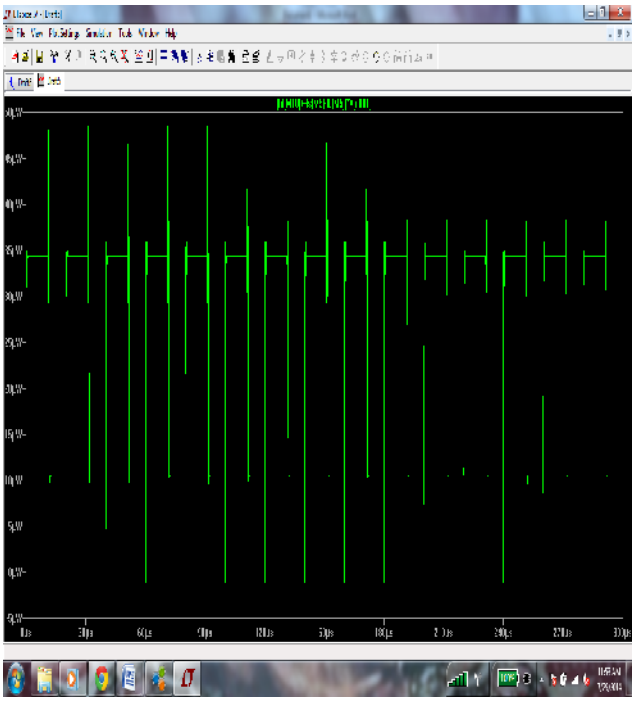

Fig. 9. Power consumption differential pair during static condition.

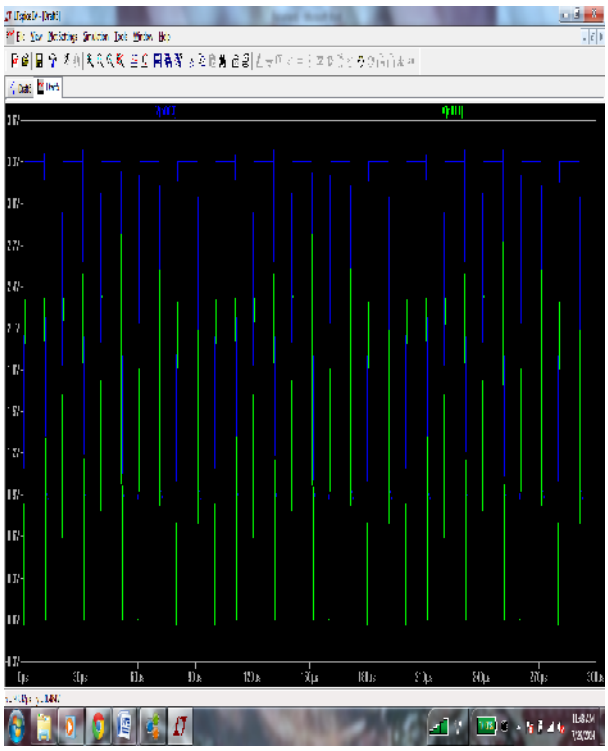

Fig. 8. Current at trail end of PMOS & NMOS differential pair.

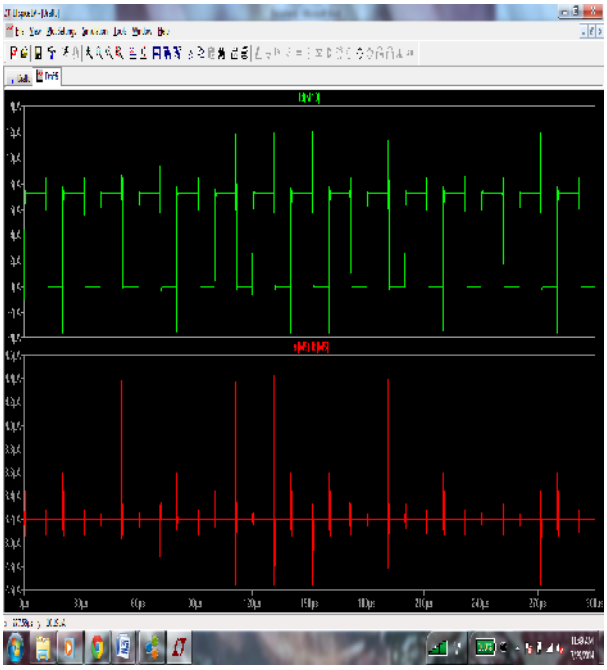

Fig. 10. Static current in biasing network and differential pair.

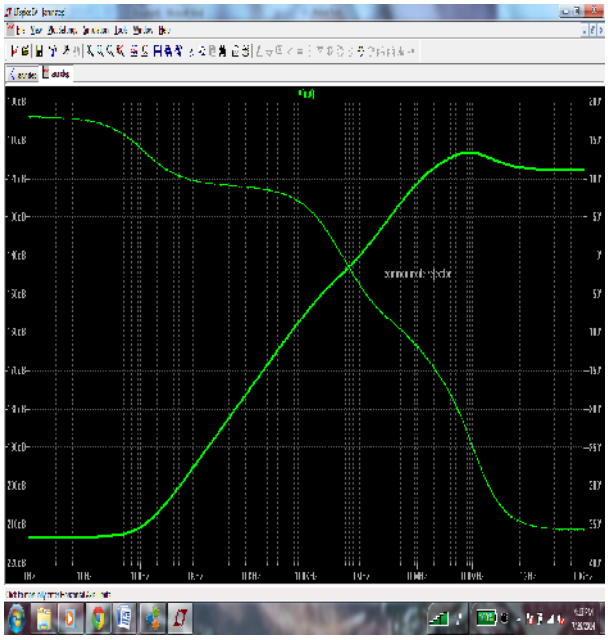

Fig. 11. Simulation result of common mode rejection ratio.

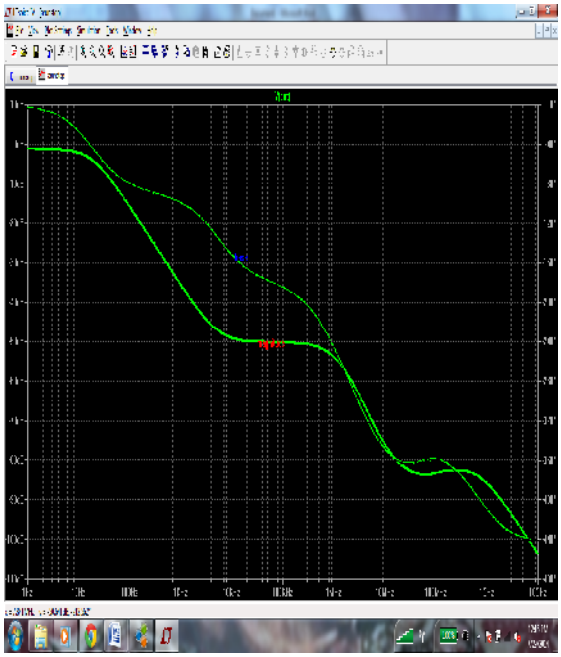

Fig. 12. Frequency response of proposed buffer amplifier.

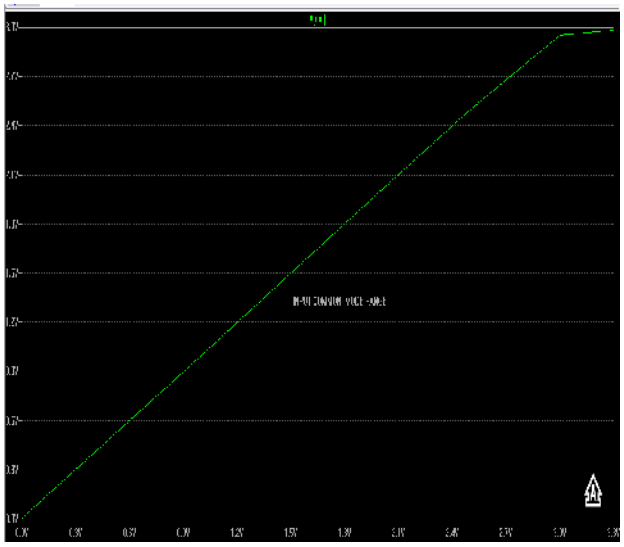

Fig. 13. Simulation result of Input common mode range.

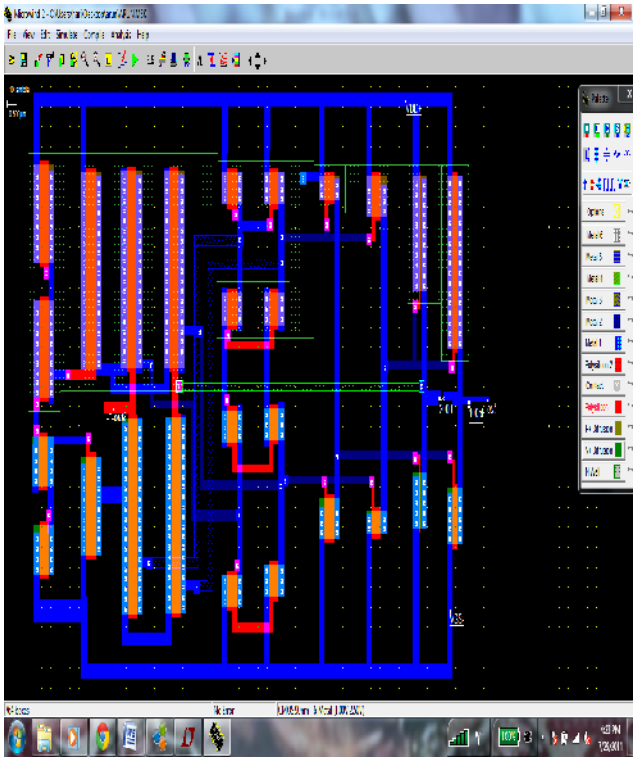

Fig. 14. Layout diagram of rail to rail differential amplifier.

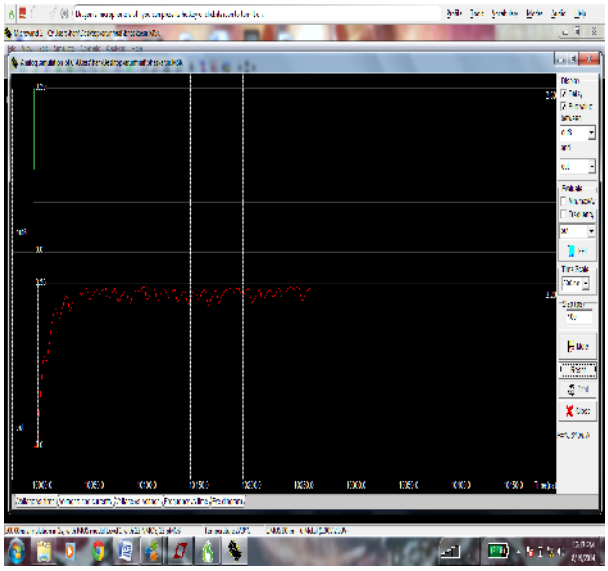

Fig. 15. Simulation result of rail to rail differential amplifier for step response.

VII. COMPARISON TABLE

	Ref.[20]	Ref.[3]	Ref.[4]	Ref.[1]	This work is
CMOS technology	.6 µm	.6 µm	.6 µm	.5 µm	.35 µm
Supply voltage	5 V	5 V	5 V	5 V	.33 V
Max load capacitor	680 pF	170 pF	30 pF	1000 pF	1000 pF
Quiescent current	30 µA	5 µA	8.2 µA	32 µA	8 µA
Settling time	1.2 µs	9.6 µs	8.2 µs	.7 µs	3.2 µs
Input-output range [V]	.15/4 V	.15/4.8 V	.5/4.5 V	0/5 V	0/3.2 V
Input-output range [VDD%]	77%	93%	80%	100 %	97 %
Slew rate	–	–	–	–	7 V / µs
Active area [µm^2]	N/A	N/A	N/A	73 × 91	50 ×60

VIII. CONCLUSION

Self biased high-speed low-power rail to rail buffer amplifier for LCD is proposed work under class B operation which is suitable for small and large size LCD panel, the Zero compensation is used to enhance the slew rate and settling time the compensation resistor value should be optimized to get the optimal value of slew rate and phase margin, as with large value of compensation resistor we get adequate phase margin but it will increase settling time and vice versa. A prototype of this buffer is implemented on 0.35 µm CMOS technology it draws only is 8 µA static current. The buffer draws little static current but has a large driving capability during transition phase , full swing is obtained by RAIL TO RAIL operational amplifier and enlarge driving capability is obtained by the use of two comparators. The buffer is 3 µs of rising settling time and 3.2 µs of falling settling time, the active area occupied by the buffer is approximately 3600 μm^2. The performance of the proposed buffer is compared with previous buffer it is superior in power consumption, low static current and small settling time.

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